Lock-In Amplifier with Sub-PPM Resolution

Graduate

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Introduction: The goal of this thesis is to improve an existing digital Lock In Amplifier (LIA) measuring capacitance variations using a charge sensitive amplifier as the sensor element. The existing circuitry can measure variations of 71 parts per million (PPM). The aims are to enable sub PPM measurements, to enlarge the carrier frequency range of the LIA, to implement the digital processing on an FPGA, and to produce a PCB of the system. A previously published study presents an Enhanced Lock In Amplifier (ELIA) structure, which promises a sub PPM resolution by utilizing two measurement channels. This structure is used to design the overall system architecture.

Approach: The existing charge sensitive amplifier is modified by adding a low noise, high gain JFET amplifier stage in the signal path. Additionally, the multiplexing circuit of the ELIA (SW1 and SW2) is tightly integrated into the charge sensitive amplifier circuitry instead of being located directly in front of the ADCs. SPICE models are created for the analog signal path to evaluate its performance. Python scripts simulating the digital part of the ELIA further process the SPICE simulation output, from which a final SNR is calculated. All mathematical processing is designed to be implementable on an FPGA.

From the simulation results, a final schematic and PCB of the system is produced. The digital part of the ELIA is implemented on a Xilinx Zynq-7000 module.

Result: The simulations show promising results. A one to two PPM resolution could be achieved with the designed circuit using the ELIA technique. The SNR of a 500aF capacitance variation, which corresponds to 71 parts per million, is 38 dB. This is an improvement of 24 dB compared to the existing design.

The PCB could not be fully commissioned due to time constraints. However, the sub circuits which are operational have been evaluated for noise and functionality with real world measurements. The sub circuits noise behavior is either as specified in the datasheet, or better. The main working circuit is a two stage, second order Sallen-Key bandpass filter, which achieves the designed pass band gain of 12dB in the specified frequency range of 10kHz to 10MHz and the 40 dB per decade rise and roll of in the stop bands. The simulated pass band noise voltage density is $7nV/Hz^{1/2}$. The measured noise density is $4nV/Hz^{1/2}$ in the same frequency range. The analog power circuitry is also evaluated for noise. The noise voltage density is below $30nV/Hz^{1/2}$ between 10kHz and 1MHz.

ELIA Structure

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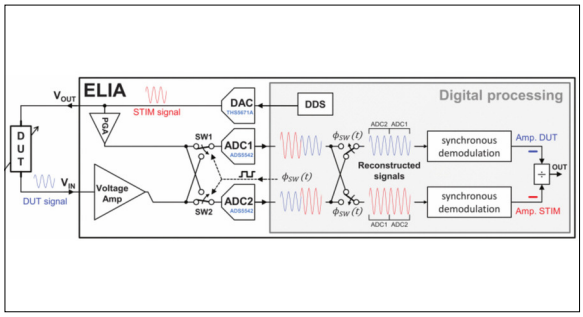
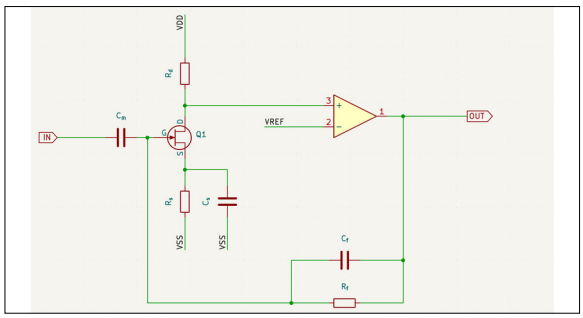
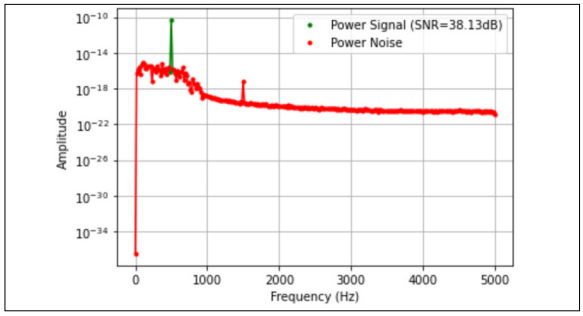


Charge Sensitive Amplifier with JFET Preamplifier
Own presentment



ELIA Output Spectrum from transient noise SPICE simulation, 71 PPM variation
Own presentment



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