

Design of a fully integrated Buck-Boost Converter ASIC

A small Buck-Boost Converter ASIC with integrated switches on a commercial 0.35 um process node

Students

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Introduction: This part of the project focuses on the post-layout phase of a project, which was divided into pre-layout and post-layout stages. The project was initiated by Sonova AG, with the objective of designing a compact 200 mA DC/DC converter for the potential integration into the charging case of their hearing devices. The device should generate a stable 5 V supply from a USB power source with an input range of 4.35 V to 5.5 V, in accordance with the USB specification. In addition to the analog circuits in the switching converter, a digital SPI interface was added which allows for digital configuration of the device settings.

Approach: During this second phase of this project, we successfully finished the chip design and were able to meet the tape-out deadline. Afterwards, in preparation to receiving the samples, we created the test setup, creating both custom hardware and software for semi-automated chip testing from scratch. This allowed us to quickly start testing and gathering data as soon as the samples arrived.

Result: The SPI interface was successfully validated with a Python driver, enabling register read/write operations to configure the chip on the fly. While the power-on reset and bandgap voltage reference were inside the specifications, the internal current reference showed a deviation of about 38.8% from the simulation. A likely cause is a not anticipated tolerance deviation in the 'rnp1' resistors used. The oscillator showed a deviation of about 54.7% from the simulation. Fortunately, both of these problems had a minimal impact and the function of the IC.

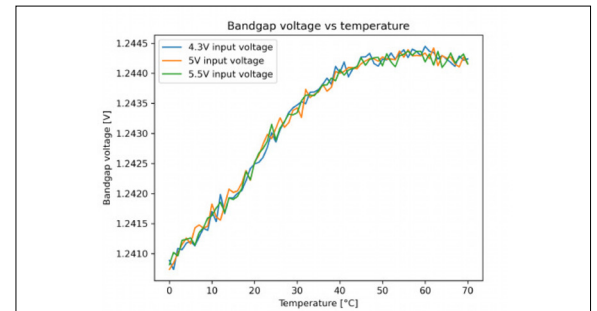
Both the response to a load step as well as the conversion efficiency of the chip are satisfactory and within the range specified. The efficiency was measured under various load conditions and with varied input voltages and can be seen in the second plot below. The converter achieves a peak efficiency of 80% at a 100mA load.

Overall, the samples characterized largely conform with the simulated values. The chips were even able to sustain loads currents of up to 300mA, an increase of 50% over the designed maximum, while maintaining correct operation.

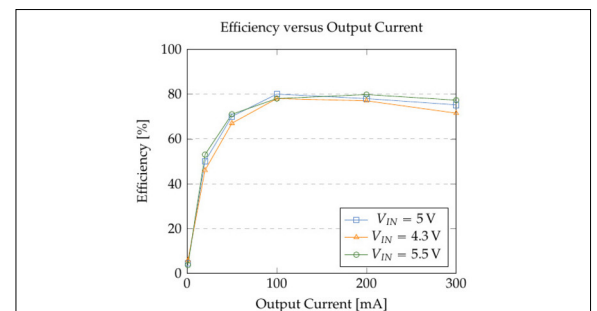
Advisor
Lars Kamm

Subject Area
Electrical Engineering

Bandgap voltage vs temperature measured
Own presentation



Conversion efficiency at frequency = 1.17 MHz; Data points for 20 mA and 50 mA are estimates based on interpolation
Own presentation



Compilation of the main measured device characteristics compared with their simulated values
Own presentation

Parameter	Information & Test Conditions	Sim	Min	Max	Unit
Buck-Boost Converter					
V _{OUT}	Average output voltage	5.01	4.99	5.03	V
V _{OUT,PP}	Ripple voltage on V _{OUT} , I _{LOAD} = 200 mA	13.2	-	200	mV
Line Regulation	V _{IN} = 4.3 - 5.5 V, I _{LOAD} = 200 mA	< 1	< 1	< 1	%
Load Regulation	V _{IN} = 5.0 V, I _{LOAD} = 0 - 200 mA	< 1	< 1	< 1	%
f _{SW}	Converter PWM frequency	1000	1170	2630	kHz
η	Efficiency @ f _{SW} = 1 MHz, I _{LOAD} = 200 mA	83.48	-	80.0	%
ω _h	Regulation loop crossover frequency	20	30	-	kHz
f _{PM}	Regulation loop phase margin	45	-	55	°
Current Consumption					
I _{Q,DDOL}	Quiescent current in V _{DDL} , V _{DDI} = 5 V, V _{BST} = 0 V	-	-	1.12	mA
I _{IN,STBY}	Input current V _{DDI} = V _{IN} = 5 V, I _{LOAD} = 0 mA	1.03	-	19	mA
I _{SH,DDOL}	Shutdown current in V _{DDI} , V _{DDI} = 5 V, V _{BST} = 5 V	-	-	< 10.0	μA
I _{LEAK,SW}	Leakage current in V _{IN} , V _{IN} = 5 V, V _{BST} = 5 V	-	-	140	μA
Miscellaneous					
V _{UVLO}	Positive-going UVLO threshold voltage	3.4	-	3.72	V
V _{FB} = V _{REF}	Internal FB reference voltage	1250	1239	1290	mV
I _{REF}	Internal reference current	10.5	14.11	14.88	μA
R _{DS(on),HS}	High-Side switch ON-Resistance	58.3	-	-	mΩ
R _{DS(on),LS}	Low-Side switch ON-Resistance	37	-	-	mΩ