Implementations for Scattering at 1.8 Volt between Battery-less Transponder and Mobile Telephones

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***Abstract*—This work concerns advanced implementations of a battery-less transponder operated by intentionally generated wireless signals in the $2.4\,\mathrm{GHz}$ ISM band. The wireless signals consist of a power supplying data stream and of a quasi-continuous Bluetooth RF (radio frequency) signal, which enables the transponder to back-scatter the RF signal to a receiver. Our setup uses two regular, unmodified mobile telephones, one for transmitting the signals, the other for receiving the scattered signals. The transponder modulates the quasi-continuous RF signal according to a subcarrier and a predetermined $1\,\mathrm{Mbit/s}$ bit-stream. The present extended study further compares advanced implementation techniques: Micro Controller Unit (MCU), FPGA (Field Programmable Gate Array), CPLD (Complex Programmable Logic Device) and ASIC (Application Specific Integrated Circuit) and implements a CPLD test version. Experimental results suggest that our CPLD is more suitable than MCU or FPGA implementations. The paper further demonstrates the transition from a fully synchronous to a low-power asynchronous CPLD implementation. The measured power consumption for generating the bit-stream is $87\,\mu\mathrm{W}$, which results in a 6-fold reduction compared to our previous work. Accordingly, the asynchronous CPLD implementation increases total efficiency by $40\,\%$ and it is expected that this will significantly extend the wireless operational range of the battery-less transponder. Thus, the CPLD technology enables fast, flexible, and cost-effective implementation, particularly in the field of research and development.**

***Index Terms*—back-scattering, battery-less, harvesting, mobile telephone, subcarrier, MCU, DMA, FPGA, CPLD, ASIC.**

I. Introduction

BATTERY-LESS transponders become increasingly important as IoT (Internet of things) devices strongly gain more attention, particularly if considered under the aspect of maintenance-free operation. One application is known from RFID (Radio-frequency Identification), which is commonly used to establish inventories of goods equipped with RFID tags. The tag information is retrievable by using an RFID reader that transmits RF (radio frequency) signals to the tag, which returns the tag information by reflecting and modulating the incident RF signal. In effect, this back-scattering technology delegates the power demanding wireless carrier signal generation from the battery-less transponder to the powerful RFID reader. However, these type of RFID readers are complex and of limited usability. On the other hand, mobile telephones are everyone's constant accompany, but are unsuitable for tag readings over more than very short distances (e.g. NFC) since the emitted RF power is typically too weak. Nevertheless, it is possible to increase the available energy at the transponder by combining RF scattering with accumulating RF energy over time (RF harvesting). For example, [1] and [2] suggest RF harvesting but require a continuous wave (CW) signal for the back-scattering such that the scattered signal is detectable by the telephone's Bluetooth Low Energy (BLE) receiver. However, a CW signal source is neither generally available nor ubiquitously usable. Therefore, our experiments focus on conventional, unmodified mobile telephones based on regular hardware and commonly programmed software: one for emitting a strong harvesting signal and a quasi-continuous signal, the other for receiving the back-scattered signals. The achievable wireless operational range is limited to a few centimeters, which motivates the present study, an extended version of [3], to evaluate possibilities of further expanding these limitations.

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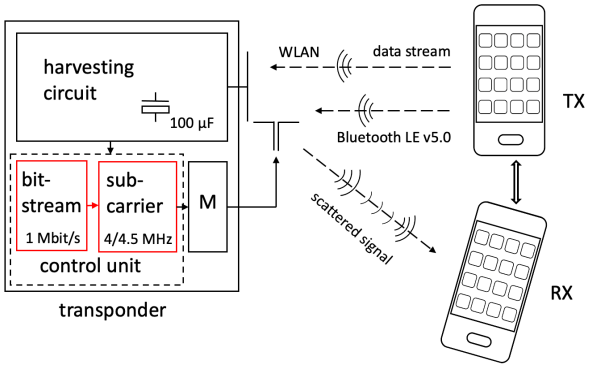

Fig. 1. Overview showing transmitter TX, receiver RX and transponder with harvesting circuit and separated bit-stream generator and subcarrier generator.

II. Background

Corresponding to our preceding work [3], Fig. 1 and Fig. 2 show the basic setup that comprises transmitting telephone TX, receiving telephone RX and a transponder with RF harvesting circuit HV (e-peas AEM30940), control unit CU and modulator M. The signal for RF harvesting consists of a continuously generated data stream transmitted via WLAN (Wireless Local Area Network, IEEE 802.11-2012). On the other hand, BLE Standard 5.0 enables extended advertising messages of $255\,\mathrm{Bytes}$ and periodic re-transmissions by using

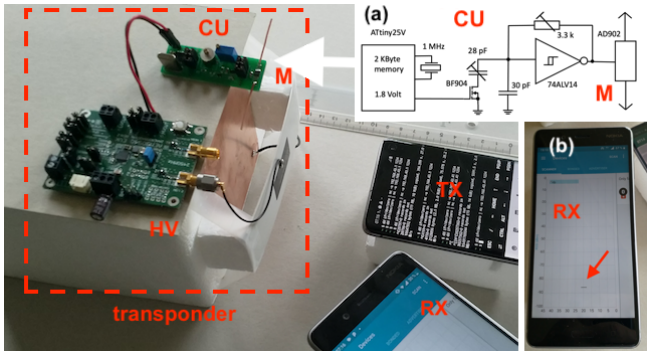

Fig. 2. Setup with mobile telephones TX, RX and transponder with harvesting HV and scattering SC units, schematics (a) and captured BLE message (b)

secondary advertising channels within the ISM band in a random-like manner. With our specifically designed messages (App on Android version 9 with Application Programming Interface API 28) we are able to produce sporadic advertising messages that appear as continuous wave signals during $2\,\mathrm{ms}$ at approx. $2475.75\,\mathrm{MHz}$. These quasi-continuous wave signals enable the scattering with a 4 and $4.5\,\mathrm{MHz}$ frequency translation resulting in scattered signals at $2480 \pm 0.25\,\mathrm{MHz}$ (BLE channel 39). The transponder of Fig. 2 operates at $1.8\,\mathrm{V}$ and comprises a MCU (Micro Controller Unit) with external crystal for generating a bit-stream ($1\,\mathrm{Mbit/s}$) and an analog RC-oscillator for generating a subcarrier signal that provides the $4/4.5\,\mathrm{MHz}$ frequency translation in dependency of the bits to be transmitted (series of $200\,\mathrm{bit}$ BLE4.2 messages + $56\,\mathrm{bit}$ pause) until the harvested energy that corresponds to the discharge voltage difference is consumed ($C{\cdot}\Delta V^2/2$). The resulting, experimental and non-standard $78\,\%$ duty cycle economizes startup procedures and speeds up BLE-message detection. The oscillator capacitance is switchable (MOSFET) for continuous-phase shifting the subcarrier frequency between $4/4.5\,\mathrm{MHz}$ in dependency of the message bits (e.g. tag ID) to be transmitted. Fig. 2b shows the event of a successfully captured BLE message at the receiving mobile telephone (red arrow). This setup reduced active power consumption from 9 to $1.12\,\mathrm{mW}$ and extended the wireless operational range from 2 to $\approx 4\,\mathrm{cm}$. The efficiency improvement extended the period of effective back-scattering during the harvesting cycles, which increased the detection probability and thus the wireless operational range. Therefore, we expect that advanced implementations will further improve power efficiency and range.

III. Technologies

All our bit-stream generator implementations use an external Temperature-Compensated crystal Oscillator (TCXO e.g. SIT1576, $5\,\mathrm{ppm}$, $16\,\mu\mathrm{A}$ @$1\,\mathrm{MHz}$ or $40\,\mu\mathrm{A}$ @$2\,\mathrm{MHz}$). Internal device oscillators are power-efficient but often lack the $50\,\mathrm{ppm}$ accuracy required by the BLE Standard. In contrast to our previously used analog RC oscillator (e.g. $322\,\mu\mathrm{A}$ @$4/4.5\,\mathrm{MHz}$), the subcarrier may be generated by an internal oscillator (e.g. ASIC) or by digitally dividing a $36\,\mathrm{MHz}$ clock signal by 8 or 9 (e.g. FPGA).

A. MCU

The MCU (STM32L0, $32\,\mathrm{bit}$ ARM Cortex-M0+) with external $2\,\mathrm{MHz}$ TCXO uses DMA (Direct Memory Access) and SPI (Serial Peripheral Interface), which allows to transfer the constant bit-stream data directly from flash memory to the SPI peripherals and to put the CPU (Central Processing Unit) into deep sleep mode after setting up the start configuration (Boot Code). This results in a power consumption of $270\,\mu\mathrm{W}$ for bit-stream generation, which is $50\,\%$ less than our preceding setup [3]. The Von Neumann architecture of the ARM Cortex-M0 prevents a lower system frequency of $1\,\mathrm{MHz}$. This disadvantage could be eliminated with an ARM Cortex-M4 core (Harvard architecture), so that the power consumption can be reduced even further.

B. FPGA

Our FPGA (Field Programmable Gate Array) considerations involve bit-stream as well as subcarrier generation by two low power FPGAs: Microchip IGLOO ($130\,\mathrm{nm}$ technology) and Lattice iCE40. Both FPGAs require an external oscillator (e.g. $2\,\mathrm{MHz}$ TCXO) and apply internal frequency multiplication (PLL) to $36\,\mathrm{MHz}$ and clock division by 8 or 9. Basic calculations show that IGLOO consumes $\approx 1.75\,\mathrm{mW}$, whereas the iCE40 requires $\approx 3.4\,\mathrm{mW}$, which is mainly related to the power hungry PLL multiplication and the divisions for subcarrier generation. Thus, these all integrating configurations seem less suitable for our application. An experimental IGLOO setup for the bitstream generation alone @$V_{bank} = 1.8\,\mathrm{V}$ and $V_{core} = 1.2\,\mathrm{V}$ is obtainable from harvesting circuit), shows a consumption of $720\,\mu\mathrm{W}$ for a shift register implementation of 256 cells (includes 56 bits for pause) and $580\,\mu\mathrm{W}$ for a ROM lookup version for $256\,\mathrm{bit}$. Consequently, a power consumption of $652\,\mu\mathrm{W}$ (inkl. $72\,\mu\mathrm{W}$ for external oscillator) is feasible, which however is clearly less efficient than the MCU solution.

C. CPLD

CPLDs (Complex Programmable Logic Device) are reconfigurable digital circuits comprising functional cells that need programming to implement the desired function. This programming changes the physical connections within and between the functional cells and external connectors. Our CPLD implementation, a Lattice ispMACH LC4032ZE ($180\,\mathrm{nm}$ technology), and its optimization is described in chapter IV.

D. ASIC

ASIC (Application-Specific Integrated Circuit) technology offers highly efficient and optimized solutions but with limited redesign flexibility and expensive prototype development. As illustrated in Fig. 3a. our simulation uses a circuit in xh018 ($180\,\mathrm{nm}$) technology from XFAB at $1.8\,\mathrm{V}$. The circuit comprises a Power On Reset (*POR*) circuit, a stop down counter (*SDC*), Read Only Memory (*ROM*) and a switchable oscillator (*SWOSC*). The $1\,\mathrm{MHz}$ clock signal may be supplied by two variants: experiment D1 from an external *TCXO* (e.g. SIT1576, which requires $16\,\mu\mathrm{A}$ and the ASIC input-cell $0.96\,\mu\mathrm{A}$) or

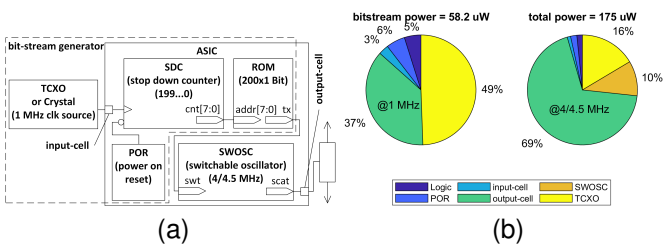

Fig. 3. ASIC: overview (a), distribution of energy experiment D1 (b)

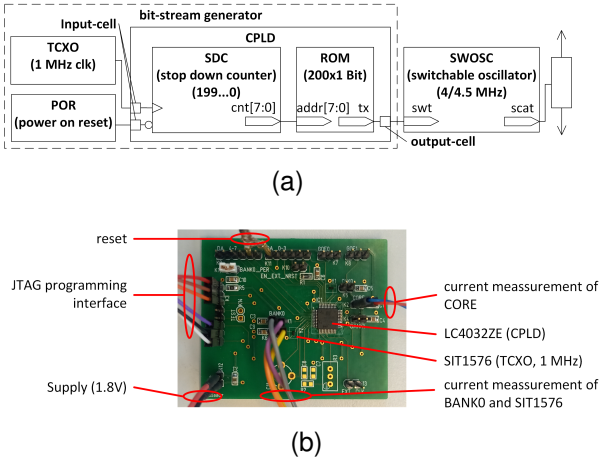

Fig. 4. Overview of CPLD implementation (a) and PCB of CPLD measurement setup (b)

experiment D2 from an ASIC-driven external crystal, requiring $95\,\mu$A, including ASIC input-cell (data sheet of Intellectual Property (IP) Block). The Post Place&Route analog transient simulation shows that the fully synchronized logic consumes $1.58\,\mu$A (@$1\,$MHz system clock), of which $0.78\,\mu$A ($55\,\%$) is for the clock tree and $1.13\,$nA for the static current. In addition, we assume that the *POR* circuit requires $1.8\,\mu$A (data sheet of IP-Block), the $4/4.5\,$MHz *SWOSC* requires $10\,\mu$A (as demonstrated in [4]) and the ASIC output-cell requires $67\,\mu$A (@$4/4.5\,$MHz with $2\,$pF parasitic load capacitance). Thus, our simulation and the external references indicate that a total power consumption of $175\,$muW is feasible (experiment D1). Alternatively, the design variant with an external crystal requires $316\,\mu$W (experiment D2). Particularly the result of our experiment D1 corresponds to the $205\,\mu$W power requirement of [2], which however operates at $50\,$MHz system clock. An asynchronous implementation as presented in chapter IV-1 (i.e. excluding the clock tree) may reduce power consumption of the logic even further.

IV. CPLD IMPLEMENTATION

Fig. 4a shows a CPLD implementation for bit-stream generation with external *TCXO*, *POR* and *SWOSC* for subcarrier generation. Fig. 4b shows the corresponding test setup for power consumption measurements. The CPLD operates at $1.8\,$V (core and bank) and upon reset, an $8\,$bit *SDC* decrements from 199_{dec} to 0 and stops at 0. The count value cnt corresponds to an address $addr$ of a 200x$1\,$bit *ROM* for providing the predetermined bit-stream at the tx output.

1) From fully Synchronized to Optimized CPLD Implementation: Total power consumption is determined by in-rush, start-up, static, and dynamic power [5]. Inrush power is given by the CPLD and its blocking capacitors. Start-up power, caused by loading the configuration, is also technology dependent. The smallest CPLD in the ispMACH series was chosen to keep the static power as low as possible. Dynamic power dissipation is generally represented by the approximation $P_{dyn} = \alpha C_l V_{dd}^2 f_{clk}$, where α is the switching activity factor (also called transition probability), C_l is the overall capacitance to be charged and discharged in a reference clock cycle, V_{dd} is the supply voltage, and f_{clk} is the clock frequency [6]. The supply voltage is given by the core voltage of this technology. The frequency at which the tx signal needs to be updated ($1\,$MHz) is also given. In order to reduce power consumption, only the number of active gates α can be reduced. The coming chapters will show how to move from a fully synchronous CPLD implementation (high α) to a low-power asynchronous variant (low α).

2) Stop Down Counter: The counters in Fig. 5 count from 199_{dec} down to 0. Once the counters reach the value 0, the $done$ signal goes HIGH, and the counter stops.

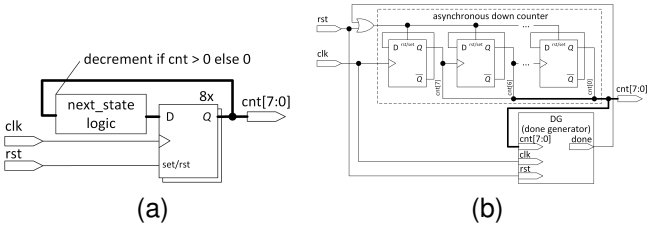

Fig. 5. stop down counter (*SDC*): synchron (a) and asynchron (b)

Fig. 5a shows a synchronous stop down counter. All flip-flops update their state simultaneously at every positive clock edge. In contrast, an asynchronous counter (Fig. 5b) works without a central clock signal. Each flip-flop changes its state based on the state of the previous flip-flop, which reduces the toggle activity. As also described in [7], this enables a current reduction of $1.9\,\%$, as the flip-flops only perform a storage process when required.

3) Done Generator: Fig. 6 shows the done generator (*DG*), which is instantiated in Fig. 5b. The circuit set the output $done = HIGH$ if the input cnt reaches 0.

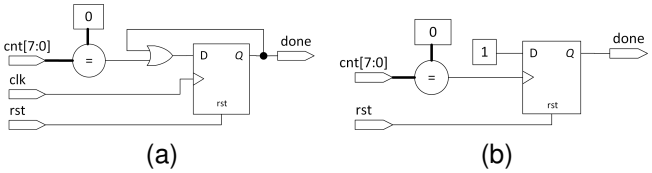

Fig. 6. done generator (*DG*): synchron (a) and asynchron (b)

As Fig. 6a shows, the $done$ signal can be stored synchronously on each clock edge. However, in order to achieve a current reduction of $4.2\,\%$, asynchronous storage as shown in Fig. 6b may be used. In this way, the flip-flop is only active when the signal cnt reaches 0 for the first time.

4) Synchronized Output Signal: As described in [8], the synthesis process of the *ROM* from Fig. 4a creates logical paths that have different propagation delays. When a signal is routed through paths with different delays, undesirable short conditions occur at the output, called hazards. The eight asynchronous output signals $cnt[7{:}0]$ of the *SDC* of Fig. 5b also promote the occurrence of hazards because they do not change at the same time. Hazards cause undesirable power consumption because the state changes are unnecessary. The power consumption increases additionally when the hazardous signal tx, as seen in Fig. 4a, is led out of the CPLD. This CPLD external line has parasitic capacitances that are unnecessarily reloaded with the output driver. As described in Fig. 7a the signal can be synchronized with the clock by interposing a flip-flop. This enables a current reduction by $27.8\,\%$, since the hazards on the signal do no longer reach the output tx of the CPLD.

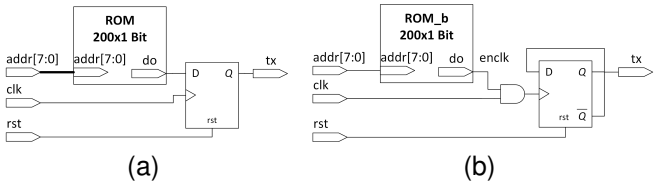

Fig. 7. circuits of synchronized output signal tx: without clock enable (a) and clock enabled toggle flip-flop (b)

5) Toggle Flip-flop with clock gating: As shown in Fig. 8a, the signal do is saved to the output tx with every positive clock edge. The flip-flop requires power for the storage process on every clock edge (dots in Fig. 8a), although the output tx does not change in every case. A circuit is now presented

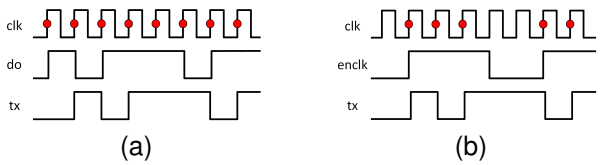

Fig. 8. synchronized output signal tx: without clock enable (a) and clock enabled toggle flip-flop (b)

in Fig. 7b that only requires power for the storage process when it is necessary. A toggle flip-flop forms the memory element that produces the output tx. The *ROM_b* stores when the toggle flip-flop should switch. Using clock enable $enclk$ and the *AND* gate, the clock signal clk is activated at the right time. Fig. 8b illustrates when the toggle flip-flop has to switch. The circuit enables a current reduction of $31.1\,\%$, as far fewer storage operations are now carried out. To convert the data D_{ROM} of the *ROM* from Fig. 7a into the data D_{ROM_b} of the *ROM_b* from Fig. 7b, use the following algorithm: $D_{ROM\_b} = (D_{ROM} \gg 1) \oplus D_{ROM}$.

6) Summary: The starting point is the fully synchronous design with a power consumption of $76.3\,\mu\mathrm{W}$. Table I shows the savings in power consumption when implementing the modifications proposed in chapter IV-2 to IV-5. The optimized design achieves a measured power consumption of $52.6\,\mu\mathrm{W}$, with a static power consumption of $29.2\,\mu\mathrm{W}$, representing $55\,\%$ of the total. Thus, these optimizations show remarkable efficiency gains and we assume that similar optimizations applied to ASICs will achieve comparable improvements.

TABLE I
DEVELOPMENT STEPS

description of development step of the CPLD implementation	**total power consumption*** [μW]	**savings** [μW]	[%]
fully synchronized implementation	76.3	-	-
chapter IV-2: asynchron stop down counter	74.9	1.44	1.9
chapter IV-3: asynchron done generator	73.1	3.24	4.2
chapter IV-4: synchronized output signal	55.1	21.2	27.8
chapter IV-5: toggle flip-flop at output signal	52.6	23.8	31.1

* total dynamic and static power consumption, averaged over 5 seconds during continuous data transmission

V. RESULTS

Table II summarizes the results of measurements (meas.) and simulations (simul.) for bit-stream generation (i.e. without *SWOSC*) to enable a fair comparison of the technologies. The MCU solution achieves a factor of 2 over our previous solution but seems less suitable for our application, presumably due to high complexity of MCU even when the CPU enters sleep mode after DMA setup. Also FPGA implementations with a general purpose architecture are unlikely to reduce power requirement. The CPLD test setup achieves a power consumption of $87\,\mu\mathrm{W}$, which is $68\,\%$ less than MCU measurements.

In our test setup as shown in Fig. 1, the WLAN transmitting power of the mobile telephone TX is limited to 20 dBm (Standard IEEE 802.11b). An external WLAN scanner (WiFi-Analyser) indicated a predominate wireless power intensity of $-32\,\mathrm{dBm}$, which results from the continuous WLAN data stream at 2427 to 2447 MHz (WLAN Channel 6). This intensity and the $100\,\mu\mathrm{F}$ storage capacitor enabled energy accumulation intervals of 5 to 7 seconds and subsequent power supplying bursts with a stable voltage of 1.8 Volt during $\approx 50\,\mathrm{ms}$. Measurements of the PCB implementation and an external crystal oscillator (ECS-2520MVLC, $260\,\mu\mathrm{W}$) achieved a wireless operational range of $5\,\mathrm{cm}$, which is still within the near-field range of the 2.4 GHz band. We expect that further harvesting and signal processing improvements will extend this to the mid-field range.

Transient analog ASIC simulations show a $33\,\%$ advantage over CPLD alternatives in generating the bit-stream (excl. switchable oscillator *SWOSC*, incl. output-cell @$1\,\mathrm{MHz}$). It is expected that a ASIC implementation similar to [2], i.e. a design with combined bit-stream generator and $4/4.5\,\mathrm{MHz}$ switchable oscillator, will reduce overall power consumption. Furthermore, we assume that optimization steps, similar to the CPLD optimizations as shown above, enable additional efficiency improvements.

TABLE II
COMPARISON OF BITSTREAM GENERATION

experiment	A	B	C	D1	D2
technology, component	MCU STM32L0	FPGA AGL030	CPLD LC4032	ASIC 180 nm	ASIC 180 nm
clock source freq. [MHz]	TXCO 2	TXCO 2	TXCO 1	TXCO 1	Crystal 1
evaluating	meas.	meas.	meas.	simul.	simul.
bit-stream Power [μW]	270	652	87	58	199

VI. CITING PREVIOUS WORK

As shown in table III, the transponder of [1] uses battery power resulting in above-mentioned maintenance problems. [2] presents an ASIC chip in $65\,\mathrm{nm}$ CMOS with an attractive active power consumption of $205\,\mu\mathrm{W}$, however this solution is inherently inflexible, expensive and time consuming and therefore less suitable in a research and development environment. Our preceding work [3] is based on unstable and power demanding discrete components, which motivates further implementation development.

TABLE III
COMPARISON OF RESULTS

reference	[1]	[2]	[3]	this work
technology, component	MCU MSP430F21	ASIC 65 nm	MCU ATtiny25V	CPLD LC4032
power supply	battery 2.5 V	external 3.5 V	RF harvest 1.8 V	RF harvest ready 1.8 V
system clock freq. [MHz]	1	50	1	1
bit-stream* power [μW]	n/a	$\approx$148	540	87
subcarrier generator power [μW]	LC osc. 12 MHz n/a	freq. div. 4/5 MHz n/a	ext. RC osc. 4/4.5 MHz 580	ext. RC osc. 4/4.5 MHz 580
total active power [μW]	1560	205	1120	667

* static + dynamic power of logic, power on reset and system oscillator

VII. CONCLUSION

MCU and FPGA solutions appear to be less suitable for our low power application because of their relative high power consumption of $270\,\mu\mathrm{W}$ and $652\,\mu\mathrm{W}$, respectively. In contrast thereto, the presently tested CPLD implementation consumes $87\,\mu\mathrm{W}$ for bit-stream generation, which corresponds to a factor of 6 reduced power consumption compared to our preceding MCU setup requiring $540\,\mu\mathrm{W}$ [3]. This corresponds to a total efficiency improvement of $40\,\%$. On the other hand, our ASIC simulations together with assumptions concerning subcarrier generation (e.g. $4/4.5\,\mathrm{MHz}$ oscillator) suggest that a total power consumption of $175\,\mu\mathrm{W}$ is feasible, which basically confirms the $205\,\mu\mathrm{W}$ as demonstrated by [2]. In the present application, the achievable wireless operational range mainly depends on the power harvesting capability and the acceptable waiting time. Nevertheless, optimizations of power consumption significantly relax these constrains, as shown by the CPLD implementation and the measured range improvement from 4 to $\approx 5\,\mathrm{cm}$. Thus, the results of this feasibility study and the measurements point towards promising advancements but also indicate principal limitations.

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BIOGRAPHY

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Paul Zbinden Paul Zbinden earned his Electrical Engineering diploma in 1987 and obtained a Doctor of Technical Sciences degree in 1993, both from ETH Zürich, Switzerland. He began his career at ETH Zürich's Signal and Information Processing Laboratory in 1987 as a teaching assistant, progressing to a research assistant and junior lecturer in signal processing. Following his PhD, he spent a year as a postdoc with Prof. G.S. Moschytz. In 1993, he joined Ascom Audiosys, later Bernafon, where he established an IC development team and pioneered their first digital hearing aid chip.
From 2004 to 2010, Paul Zbinden worked at Phonak AG, Stäfa, overseeing a joint venture with Cochlear Ltd to develop middle ear implants. In 2010, he joined the Institute for Microelectronics, Embedded Systems and Sensors (IMES) at Eastern Switzerland University of Applied Sciences, becoming its head in 2011. His current research focuses on hardware acceleration and Time-to-Digital Converters (TDC).

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